IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. When strikethrough cannot easily be perceived, or when five or fewer characters are deleted, [[double brackets]] are used to show the deletion. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered). Please AMEND claim 18 in accordance with the following:

1. (cancelled)

2. (cancelled)

3. (cancelled)

4. (previously presented) The semiconductor device according to claim 18, wherein a thickness of each of said semiconductor elements is 50 μM or less.

5. (previously presented) The semiconductor device according to claim 18, wherein each said semiconductor element is electrically connected by flip chip mounting to said respective wiring pattern.

6. (previously presented) The semiconductor device according to claim 18, wherein each said semiconductor element is electrically connected via an anisotropically conductive film to said respective wiring pattern.

7. (cancelled)

8. (cancelled)

9. (cancelled)

10. (cancelled)

11. (cancelled)

12. (cancelled)

13. (cancelled)

14. (previously presented) A semiconductor device, comprising:

a first insulating layer having vias extending therethrough;

a first conductive layer, comprising a first wiring pattern, embedded within the first insulating layer;

a second conductive layer, comprising a second wiring pattern, formed on the first insulating layer, the wiring pattern of the second conductive layer being electrically connected to the wiring pattern of the first conductive layer through the vias of the first insulating layer;

a semiconductor element embedded in the first insulating layer and electrically connected to the wiring pattern of the first conductive layer; and

a second insulating layer having a semiconductor element, electrically connected to the wiring pattern of the second conductive layer, embedded therein and embedding further therein the second conductive layer.

15. (cancelled)

16. (previously presented) The semiconductor device according to claim 14, wherein one or more of the wiring patterns of the first conductive layer is/are electrically connected to one or more of the wiring patterns of the second conductive layer through corresponding said vias.

17. (previously presented) A semiconductor device, comprising:

a substrate;

a first set of conductors comprising a first conductive layer formed on the substrate;

a first insulating layer formed on the first set of conductors and having vias extending therethrough, the first insulating layer having at least one semiconductor element and the first set of conductors embedded therein;

a second set of conductors comprising a second conductive layer formed on the first insulating layer and extending through vias therein; and

a second insulating layer formed on the second set of conductors and having vias extending therethrough, the second insulating layer having at least one semiconductor element and portions of the second set of conductors embedded therein;

wherein one or more of the first set of conductors is/are electrically connected to the at least one semiconductor element embedded in the first insulating layer and one or more of the second set of conductors is/are electrically connected to the at least one semiconductor element embedded in the second insulating layer and through corresponding said vias to one or more of the first set of conductors.

18. (currently amended) A semiconductor device, comprising:

a substrate having a main surface;

a plurality of device layers stacked in succession on the main surface of the substrate, wherein each of the plural device layers ~~stacked, in succession, on the main surface of the substrate, each device layer comprising~~comprises:

a set of ~~conductive layer~~conductors comprising a wiring pattern, and

~~a semiconductor element electrically connected to the wiring pattern, and~~

~~a single~~an insulating layer formed on and embedding the set of conductors and having vias extending therethrough, ~~respectively associated with~~ and embedding therein ~~the~~ a semiconductor element ~~and the respective conductor layer having conductive vias extending therethrough~~, and

wherein a wiring pattern of a first device layer is electrically connected to a first semiconductor element embedded in a first insulating layer with a first set of conductors and one or more of a second set of conductors is/are electrically connected to the first semiconductor element embedded in a second insulating layer and through corresponding said vias to one or more of the first set of conductors. ~~the wiring pattern of the conductive layer of each successive, stacked device layer being formed on an upper main surface of the single insulating layer of the respective, underlying device layer and respective said wiring patterns of the conductive layers of the plural stacked device layers being selectively electrically interconnected through the corresponding vias of the respective, single insulating layers of the stacked, plural device layers.~~

19. (previously presented) The semiconductor device according to claim 18, wherein:

the semiconductor elements are commonly disposed within the respective insulating layers and aligned in the plural, stacked device layers.

20. (previously presented) The semiconductor device according to claim 18, further comprising:

plural semiconductor elements in each of the plural device layers and commonly disposed therein so as to be in aligned relationship in the stacked layers.

21. (previously presented) The semiconductor device according to claim 18, wherein each insulating layer surrounds and covers substantially all of each outer surface of the semiconductor element embedded therein.